

LESSON PLAN

Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
1	17/10/13	Embedded systems overview design challenge Processor technology	I	Black board		
2	18/10/13	IC technology, Design Technology, Single purpose processors RT level	"	"		
3	19/10/13	Sequential logic (RT level) Custom single purpose processor design (RT level)	"	"		
4	24/10/13	Optimizing custom single purpose processors	"	"		
5	25/10/13	Basic architecture of GPP, operation, pipelining	"	"		
6	26/10/13	Programmer's view, Development environment	"	"		
7	31/10/13	ASIPs - microcontroller Digital signal processors	"	"		
8	1/11/13	State machine & Concurrent process models: Introduction models vs languages	II	Black board		
9	2/11/13	FSMD, using state machines	"	PPT		
10	7/11/13	PSM, concurrent process model	"	"		
11	8/11/13	Concurrent processes communication among processes	"	"		
12	9/11/13	Synchronization among processes, Implementation	"	"		
13	14/11/13	Data flow model, real-time systems	"	Black board		
14	15/11/13	Communication Interface: need for communication interfaces	III	"		
15	16/11/13	RS 232/UART RS422/RS485	"	PPT		
16	21/11/13	USB, Infrared	"	"		
17	22/11/13	IEEE 1394 Firewire Ethernet	"	"		
18	23/11/13	IEEE 802.11	"	"		
19	28/11/13	Bluetooth	"	"		
20	29/11/13	Embedded RTOS concepts Architecture of kernel	IV	Black board		

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21	30/1/13	Tasks and Task scheduler	"	Black board		
22	4/12/13	Scheduling algorithms	"	"		
23	5/12/13	Interrupt service routines semaphores,	"	"		
24	6/12/13	Mutex Embedded/RTOS Concepts II: Mailboxes,	V	"		
25	7/12/13	message queues, Event Registers	"	"		
26	13/12/13	Pipes, Signals. Concepts III: Timers	V	"		
27	19/12/13	memory management priority Inversion problem	"	"		
28	19/12/13	Embedded OS - Embedded Linux	"	"		
29	24/12/13	Real time OS - RT Linux	"	"		
30	28/12/13	Hand held OS - windows CE	"	"		
31	29/12/13	Design technology: Introduction	V	"		
32	20/12/13	Automation, synthesis	"	"		
33	21/12/13	Parallel evolution of compilation and synthesis	"	"		
34	25/12/13	Logic synthesis RT synthesis	"	"		
35	26/12/13	Behavioral synthesis System synthesis	"	"		
36	27/12/13	h/w-s/w co-design	"	"		
37	28/12/13	Verification	"	"		
38	2/1/14	H/w-s/w co simulation	"	"		
39	3/1/14	H/w-s/w co-simulation	"	"		
40	4/1/14	Review of Intellectual Property codes.	"	"		